Tanta University	**Second Term – Final Exam**
Faculty of Engineering	**Subject: Computer Architecture**
Computer and Control Dep.	**Allowed Time: 3 Hours**
Second Year	**Date: June 07, 2010**

Number of Pages: 2
Total Marks: 90

Attempt the following 3 questions

Question 1: [Computer Arithmetic] — 40 Marks

1. Show how you can find the number of logic gates that are needed to build 4-bit carry-lookahead adder.

(6 Marks)

2. Design 64-bit adder that uses 4 carry-lookahead adders along with additional logic gates to generate c_{16}, c_{32}, c_{48}, and c_{64} from c_0 and G_i^{II} and P_i^{II} variables. Then find the gate delay for s_{62}, s_{63}, and c_{64}.

(14 Marks)

3. Multiply the following signed 2's complement numbers using Booth algorithm and the bit pairing recording of multipliers. Assume that A is the multiplicand and B is the multiplier.

A = 01000111 B = 10100111 using:

(8 Marks)

4. Assume that the floating-point number is represented in 16-bit format with one sign bit, six bits for the exponent, and nine bits for the mantissa. Follow the same rules applied in the IEEE standard format for floating-point numbers to represent the following numbers: +1.7, -19.0, and 0.125. Then find the smallest and largest numbers represented in this format.

(12 Marks)

Question 2: [Input/Output Organization] — 30 Marks

1. Three devices A, B, and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being serviced. Suggest a suitable design for each of the following cases:
   (a) The computer has one interrupt-request line.
   (b) The computer has two interrupt-request lines, INTR1 and INTR2, with INTR1 having higher priority.

(12 Marks)

2. Design a centralized bus arbitration system that applies daisy chain between 4 I/O devices assuming that all control devices are active high. Then draw the time sequence of signals that transfer the bus mastership to device number 2.

(6 Marks)

3. Interrupts and bus arbitration require means for selecting one of several requests based on their priority. **Design a circuit** that implements a rotating-priority scheme for four input lines, REQ1 through REQ4. Initially, REQ1 has the highest and REQ4 the lowest Priority. After some line receives service, it becomes the lowest priority line, and the next line receives highest priority. For example, after REQ2 has been serviced, the priority order, starting with the highest, becomes REQ3, REQ4, REQ1, REQ2. Your Circuit should generate four output grant signals, GR1 through GR4, One for each input request line. One of these outputs should be asserted when a pulse is received on a line called DECIDE.

(12 Marks)

Question 3: [Basic Processing Unit] 20 Marks

1. Write the sequence of control steps required for the bus structure (single-bus organization of the data path inside the processor) for each of the following instructions:
   i. Add the (immediate) number NUM to register R1.
   ii. Add the contents of the memory location whose address is at memory location Num to register R1.

(10 Marks)

2. Assume that a memory read or write operation takes twice time as one internal processor step (τ) and that both the processor and the memory are controlled by the same clock. Estimate the execution time of each instruction.

(10 Marks)

Good Luck *Dr. Tarek El.Ahmady El.Tobely*